

Micro Nano Technology Visualization (MNTV) of Micromachined MEMS Polysilicon Structures

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ABSTRACT

Micro-Nano Technology Visualization (MNTV) is critical to studies in MEMS reliability. The ability to see and characterize the microstructures and interfaces with high resolution at the microscale and nanoscale is invaluable. In this paper we present the motivation, paradigm, and examples of visualization techniques applied to several aspects of surface micromachined polysilicon structures. High resolution cross-section imaging, using both a FIB/SEM and FIB/STEM, is used to acquire information on profile differences between fabrication facilities and grain size and orientation. The AFM is used to compare surface roughness of both sides (top and bottom surfaces) of thin film polysilicon after release etching. The data gathered will be extremely useful feedback for fabrication facilities in terms of process characterization and quality assurance. The data will also be useful for MEMS CAD tools where device and process models must be validated.

Keywords: MEMS reliability, MEMS visualization, process validation

1. INTRODUCTION

The MEMS field is growing extremely quickly in the new millennium. This is an exciting time, as MEMS is being thrust into the forefront of modern technology. The applications for MEMS include automotive, data storage, military (weapons systems and battlefield environments), and space (micro-satellites) to name a few. In the 21st century, critical areas for MEMS technology infusion include communications and medicine. According to a recent market analysis done by the Nexus Task Force, the total world market for microsystems is expected to grow from \$14 billion to \$38 billion by the year 2002. The market for the products identified in the study will grow at an average rate of 18% per year. From 1998 to 2002, new products under development will emerge that will contribute to even larger market growth [1].

This exponential growth expected of microsystems technology is an indication of the urgent need for microsystems reliability assessment. Reliability data gathered from all stages of device development (such as material characteristics of commercially fabricated thin films, the effect of microstructure release on device performance, etc.) will be used to improve and validate the simulation models, device designs, and fabrication processes. Thus, the simulations will be more accurate, fewer design iterations will be required, and overall development cost and

time will decrease. The required task at hand is to establish the tools and methods to thoroughly and systematically characterize MEMS fabrication processes, devices, and systems. MEMS products will then be more reliable and MEMS device development will be more efficient and less costly. These factors will promote commercialization and ultimately advance the entire microsystems technology field.

In terms of MEMS reliability concerns, efforts need to be directed at all levels in product development starting from the materials used for fabrication all the way up to system and environmental metrology. Key issues to be addressed are summarized in Table 1. As shown, there are many details that must be studied and verified to fully understand the MEMS devices being produced today. MEMS devices need to be qualified by using a unified, standardized tool set and protocol for device and process characterization.

Table 1. Summary of MEMS Reliability Issues

Topic/Property to be Investigated	Details
Material properties	<ul style="list-style-type: none"> • Residual stress • Fracture/failure mechanisms • Elastic modulus • Poisson's ratio • Fracture toughness • Electrical properties (migration, etc.) • Interfacial strength • Coefficient of thermal expansion (CTE)
Fabrication variations, manufacturing	<ul style="list-style-type: none"> • Doping • Etching parameters • Deposition methods, parameters • Post-process release etching • Post-process drying method (stiction)
Device-level metrology	<ul style="list-style-type: none"> • Grain size • Surface roughness • High resolution cross-sectioning • Microscale crack propagation visualization • Real time performance (movement) visualization • Device design effects (corners, etch holes, etc.) • Mean time to failure
Environmental effects	<ul style="list-style-type: none"> • Storage, moisture (humidity) effects • Radiation tolerance • Chemical exposure effects, contamination • Biocompatibility • Effects of extreme heat or cold • Effect of shock
System-level issues	<ul style="list-style-type: none"> • Packaging effects • Support electronics, noise • Fatigue and long term operation effects • Mean time to failure

The current state of MEMS reliability assessment is fragmented and limited. There is no cohesive effort or center that deals solely with the reliability of microstructures and microsystems. Reliability data cannot be correlated between foundries or to device design. The statistical results required for accurate risk assessment have not been obtained. Fabrication process parameters drift over time, and no attempt has been made to fully characterize and

quantify these changes or record the history of any particular process. Although industry addresses reliability issues as they become important to their product lines, many industries lack the resources (time, expertise, facilities) to do a comprehensive reliability assessment of their products. Furthermore, most reliability analyses ignore defects and nonlinearities and assume the material is homogeneous and isotropic. Reliability issues are also being addressed at various universities. For example, the mechanical properties of polysilicon (strain, Young's modulus, and fracture strength) have been characterized in air on a custom built test set-up [2]. The phenomenon of surface micromachined polysilicon layers sticking to the substrate after release etching ("stiction") has been studied and attempts to combat stiction include self-assembled monolayers and the use of lasers [3] [4]. While efforts like these are important contributions to the field, testing is not standardized and comparisons from process to process, or lab to lab, cannot be made.

Micro-Nano Technology Visualization (MNTV) is critical to MEMS reliability studies. The ability to see and characterize the microstructures and interfaces (both physically and chemically) with high resolution at the microscale and nanoscale is invaluable. MNTV, combined with other standard characterization techniques, will provide accurate mechanical data that can be used in device modeling, commercial fabrication processes that are fully characterized, and long-term reliability data such as mean time to failure. Ideally, MNTV will become part of a standardized test protocol for MEMS reliability and quality assurance assessments.

MNTV techniques include visual evaluation methods such as the use of focussed ion beam (FIB) for high-resolution cross-sectioning and metrology. Assessing release methods can be achieved with micro- and nano-scale metrology on the surfaces of test structures to determine chemical composition and topology of the remaining residues. The environmental scanning electron microscope (ESEM) is used for controlled environmental evaluation of device performance. New hardware modules will be added to the ESEM to adapt it for real-time nanoscale 3D visualization of microstructures. This type of data is useful for viewing contact angles with high fidelity (such as in MEMS optical switches), real time dry-phase etching (such as XeF_2 etching of bulk silicon), or microstructure heat evolution in liquids. A laser vibrometer may be employed for real time visualization of microstructure movement. Standard test structures, such as cantilever beams, will be used to evaluate material properties. This is particularly useful when comparing similar materials from different sources, such as polysilicon from two separate foundries.

Conclusions can then be drawn from all the data collectively. All the topics in column 1 of Table 1 are linked. For example, metrology and material properties data will have a strong correlation to device performance. The data gathered from these experiments will be extremely useful feedback for the device fabrication process. Furthermore, MEMS Computer Aided Design (CAD) tools will benefit from this data in terms of device models and simulation parameters. We intend to work closely with fabrication facilities and MEMS CAD developers to provide them with this data. The overall process flow is shown in Figure 1. Ultimately, the entire MEMS community can benefit from these studies, as the data on process validation and effects on device performance will be useful to any MEMS designer.

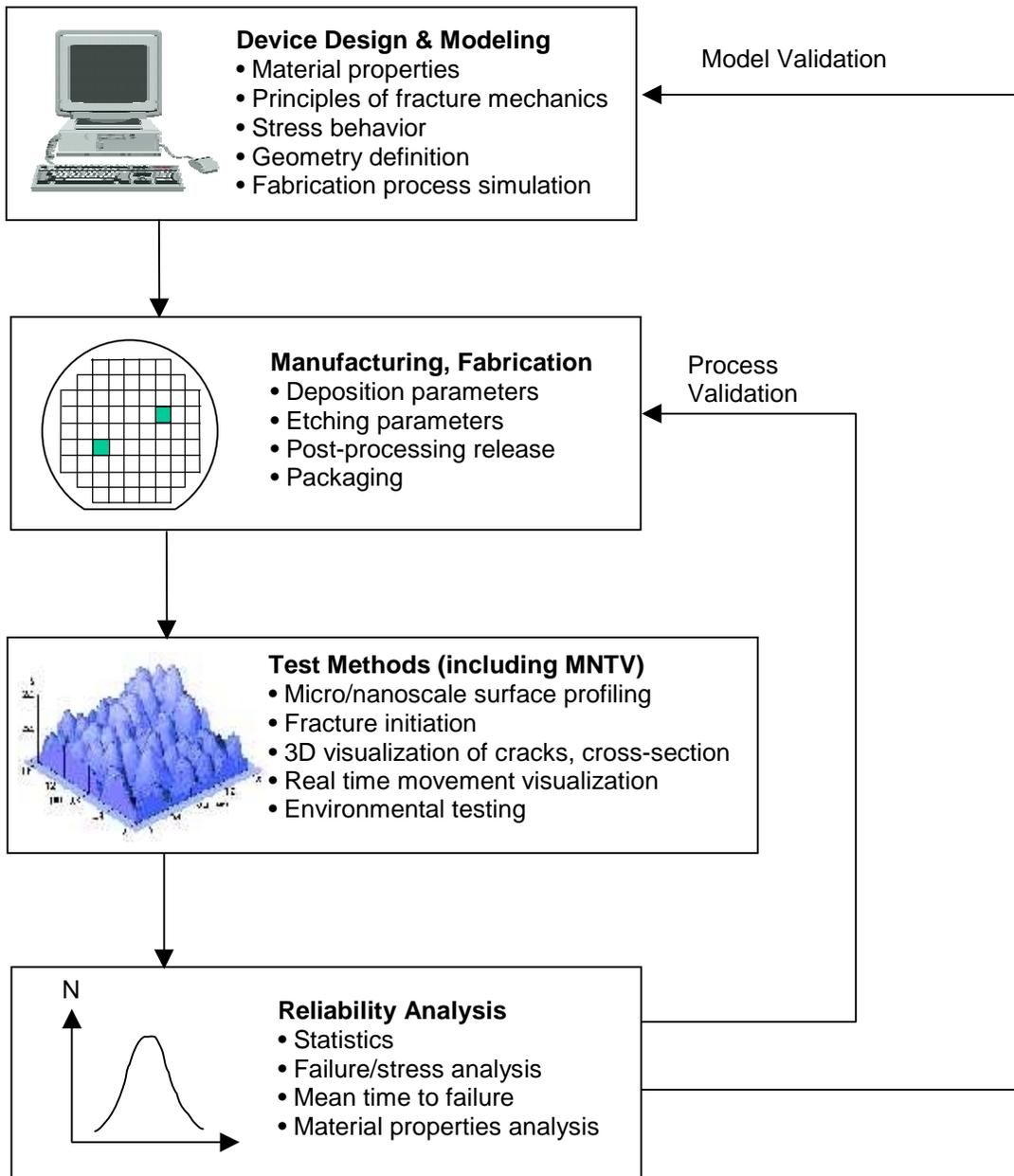


Figure 1. Diagram illustrating the systematic information flow proposed in this program. Reliability and data from all stages of the development process will be used to improve the simulation models, device designs, and fabrication process. Thus, the simulations will be more accurate, fewer design iterations will be required, and development costs will decrease.

2. CROSS SECTION METROLOGY

The focus of this paper is on the application of MNTV techniques to surface micromachined polysilicon structures. A commercially available process that we are actively characterizing is the MUMPs™ process offered by JDS Uniphase [5]. The layer stack of this MEMS-based process is shown in Figure 2. This process offers two structural layers of polysilicon (poly1 and poly2) and two sacrificial layers of silicon dioxide (oxide1 and oxide2). The poly0 layer is used as an electrical ground plane rather than a structural layer. Patterning the layers is done via photolithography and reactive ion etching.

The oxide layers are considered "sacrificial" layers because they do not appear in the final structure. When the chips come back from the foundry, the oxide is etched, freeing the polysilicon layers and allowing them to move. The required etchant is liquid 49% hydrofluoric acid (HF) which has very high selectivity for oxide over silicon and polysilicon. Proper drying of the chip after release is important to reduce the possibility of stiction. There are many methods to dry the chips, such as supercritical carbon dioxide drying [6].

Metal (0.5 μ m)
Poly #2 (1.5 μ m)
Oxide #2 (0.75 μ m)
Poly #1 (2 μ m)
Oxide #1 (2 μ m)
Poly #0 (0.5 μ m)
Nitride (0.5 μ m)
Silicon Substrate

Figure 2. MUMPs™ layer stack. Poly1 and poly2 are structural polysilicon layers, while the oxides are sacrificial layers. Poly0 is used as a ground plane and the nitride is used for electric isolation. Metal layer on top (gold) is for optional contact metalization.

CAD software tailored to MEMS design in polysilicon surface micromachining processes is commercially available [7]. In using this software, the designer can simulate process flows and view cross-sections of devices before they are actually fabricated. The cross section of a poly1 contact to a poly0 ground plane was simulated using the parameters and layer thicknesses of the MUMPs™ process (Figure 3). As shown, the conformal coverage of the polysilicon is represented as well as the relative thicknesses of each of the layers.

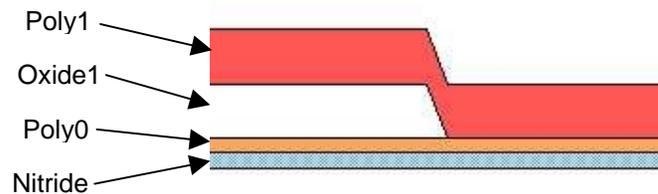


Figure 3. Simulated cross-section of a poly1 contact to a poly0 ground plane.

Process integrity is essential to successful MEMS device fabrication and can be assessed by several key metrics. In addition to accurate simulation tools, an accurate measurement of layer thicknesses and profiles is extremely important, and a comparison between simulation and experimental values must be done. Traditionally, device cross-section images are obtained by cleaving the wafer through the device, mounting the wafer in a specially designed chip holder, and imaging the cleaved area using a scanning electron microscope (SEM). This procedure can be quite destructive and hundreds of devices may be sacrificed. With a focussed ion beam (FIB) system, these measurements can be taken without the need for special chip holders or wafer cleaving [9]. A dual beam FIB/SEM uses a gallium ion beam to mill a portion of the device and an electron beam to produce a high resolution image of the device cross-section.

Images were obtained from identically fabricated, unreleased chips from two non-commercial fabrication facilities running surface micromachining processes similar to the MUMPs™ process. As shown in Figure 4, the cross-sections are dramatically different. The oxide in Figure 4(a) has sloping sidewalls compared to that in Figure 4(b). Furthermore, the oxide in Figure 4(b) was not completely etched. The thin sheet of oxide separating the first and second layers of polysilicon will cause second layer to detach from the first layer during the release etch (a catastrophic failure). These results may be due to different material properties of the oxides or differences in the RIE hardware and/or RIE plasma chemistries. In comparing Figure 3 and Figure 4, it is clear that the simulated cross section indicates a thinning of the polysilicon as it steps over the oxide layer. From the FIB/SEM photos of actual cross sections, the polysilicon does not become thinner as it covers a step in the oxide. Furthermore, it may even become thicker as shown in Figure 4(b).

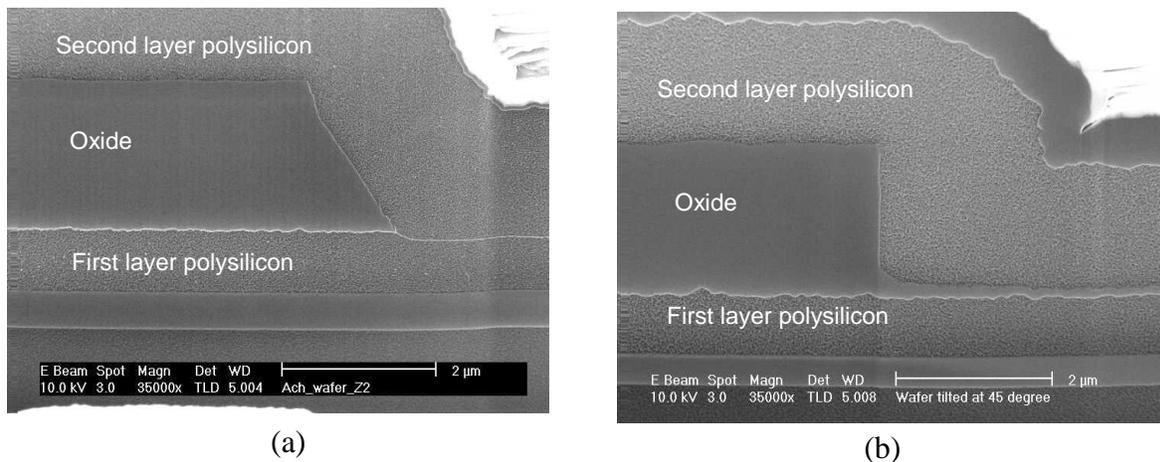


Figure 4. FIB/SEM cross-sections from chips fabricated at two separate non-commercial fabrication facilities running surface micromachining processes similar to the MUMPs™ process.

3. POLYSILICON GRAIN VISUALIZATION

Once a sample is cross-sectioned by the focussed ion beam (FIB) system, additional types of micro- and nano-scale visualization can be done. By analyzing the cross-section using scanning transmission electron microscopy (STEM), images of grain boundaries can be obtained. This information can be directly correlated to processing parameters. In terms of process control, grain size and orientation information is extremely useful.

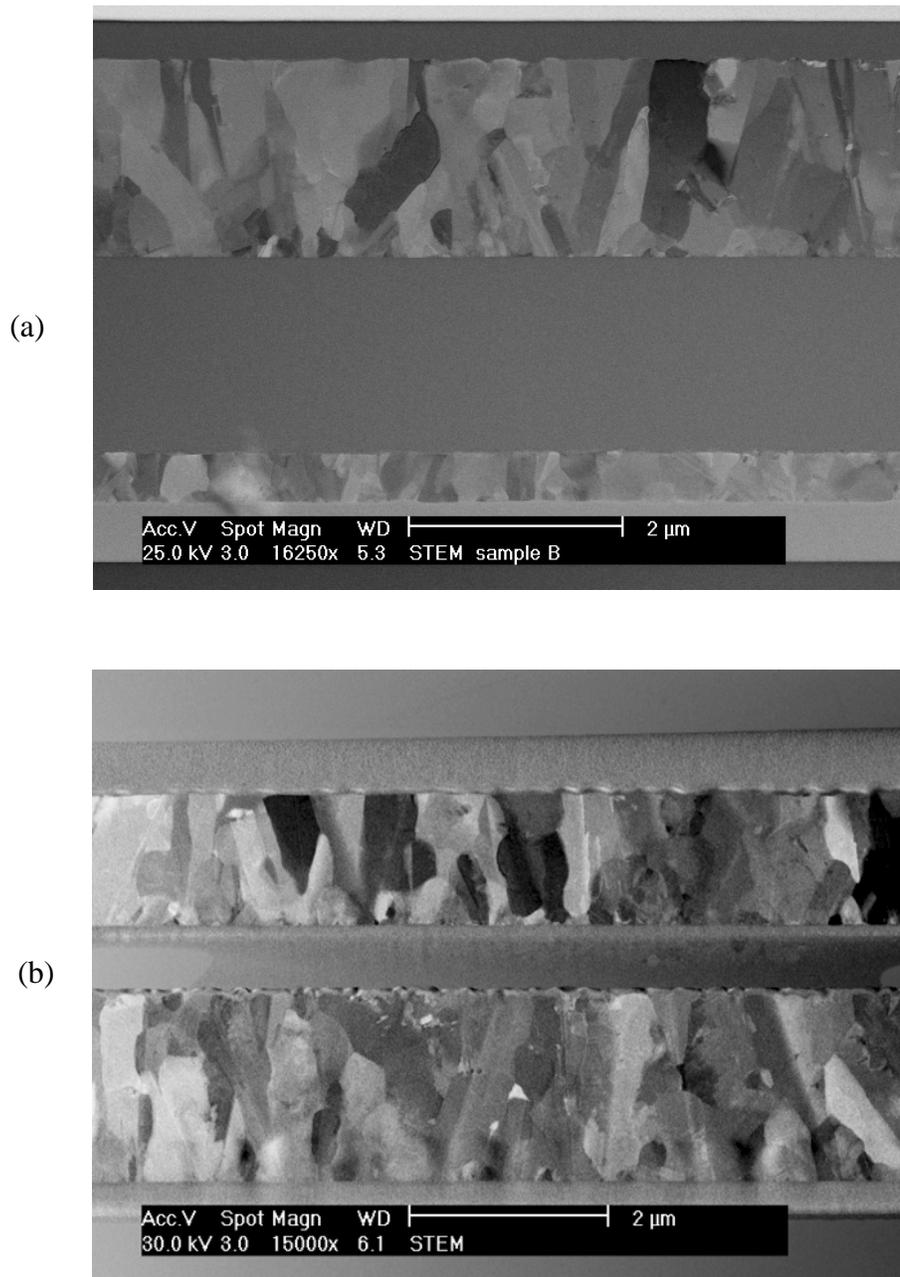


Figure 5. FIB prepared STEM images of the polysilicon layers in the MUMPs™ process. (a) STEM image of poly0 and poly1 layers before release etching. (b) STEM image of poly1 and poly2 layers after release etching. Images were taken from two separate chips.

As shown in Figure 5, the grain structure of MUMPs™ polysilicon is oriented perpendicular to the substrate. The width of the grains is roughly 1/4 - 1/3 of a micron and as much as 2μm in height. Visualization of the grain structure before and after release etching yields new insights on the effects of the etching and the quality of the release. For example, on one device a thin layer of material located between poly1 and poly2 was found. The material was crystalline in nature but did not extend all the way through the gap between polysilicon layers. The crystals were attached to the poly2 layer, and may have been the result of a reaction of the HF with the oxide or a redeposit of some unknown material from the etch bath. Further characterization of these crystals is being performed.

In general, grain orientation information is vital to fabrication process control, particularly in the validation of film deposition parameters such as time and temperature. Grain orientation will have an effect of surface morphology which will influence device performance, especially in devices where surfaces must contact each other. Surface morphology can be accurately characterized using other MNTV techniques, as described in the next section.

4. ATOMIC FORCE MICROSCOPY

Atomic Force Microscopy (AFM) is a visualization tool that allows the user to resolve surface roughness on the nanoscale. The AFM was used to image both sides of a poly1 plate from the MUMPs™ process. Specifically, a poly1 plate test structure was drawn using MEMS CAD software [7]. It was designed with polysilicon microhinges along one side such that the plate could be rotated 180° after release etching [8]. Once the plates were released, several were manually rotated and secured to the substrate using tungsten needle probes at a probe station. The AFM, in tapping mode, was then used to scan a small area of the rotated plates as well as the non-rotated plates. Thus, both sides of the polysilicon (the top surface and the underlying, bottom surface) could be scanned.

The results of the scans are shown in Figure 6 and Figure 7. Both scans are shown on the same scale for comparison. The data indicates that the top surface of the polysilicon is rougher than the bottom surface. For the specific plate scanned in the figures, the average surface roughness for the bottom surface is 1.54nm and the root mean square roughness is 1.97nm. The peak to valley deviation is 25.6nm. The corresponding average surface roughness for the top surface is 7.20nm and the root mean square roughness is 9.05nm. The peak to valley deviation is 66.7nm. The data was consistent over four separate poly1 plates. This data can be correlated to the grain orientation data in the previous section. Since the grains are forming perpendicular to the surface, it is expected that the top surface would be rougher than the bottom surface. Further characterization is being performed on unreleased chips to analyze the morphology effects of release etching at the nanoscale.

5. OTHER VISUALIZATION TECHNIQUES

In addition to cross-sectional SEM imaging, STEM, and AFM, there are numerous other aspects of reliability and quality assurance such as *in-situ* process monitoring during deposition/layer growth, device performance, residual stress measurements, and the use of custom integrated MEMS testing benches for more complicated analyses [10]. Raman scattering is a second-order inelastic scattering process. The incident light, provided by a laser, is used to excite optical phonons and is focused on the sample through a cylindrical lens (macro-Raman spectroscopy) or through a microscope (micro-Raman spectroscopy or "μRS"). The μRS technique can be used to analyze chemical composition and crystallinity with μm precision [11]. The Raman frequency depends on composition and the peak is affected by crystallinity. Recently, this technique has been used for local stress studies in thin films. Mechanical strain or stress will affect the frequencies of the Raman modes and shift the intensity peaks of the spectra [12]. *In-situ* measurements of process monitoring, such as the annealing of silicon - the Raman peak grows as annealing takes place, indicating a change in the silicon crystal structures. Temperature can be measured in a similar fashion.

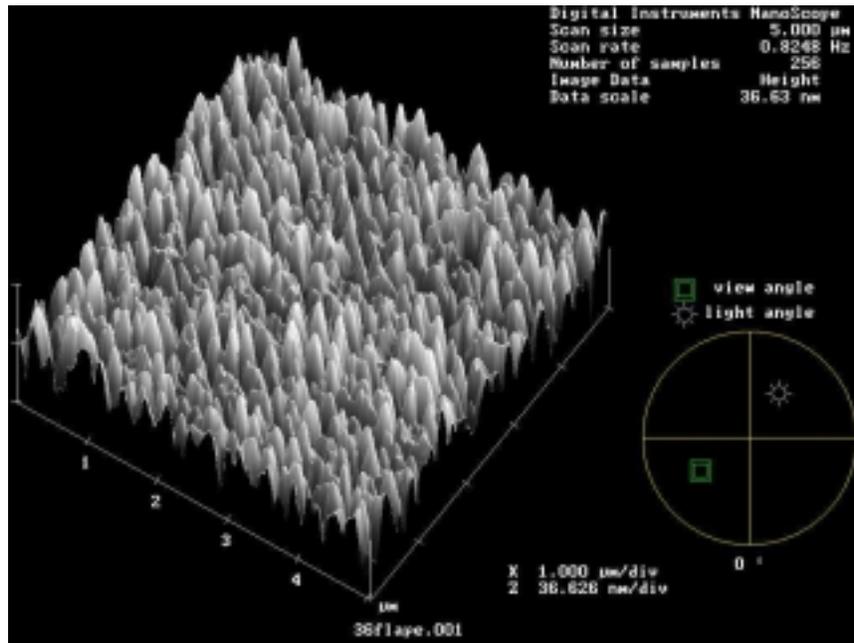


Figure 6. AFM scan of the top surface of a released poly1 plate.

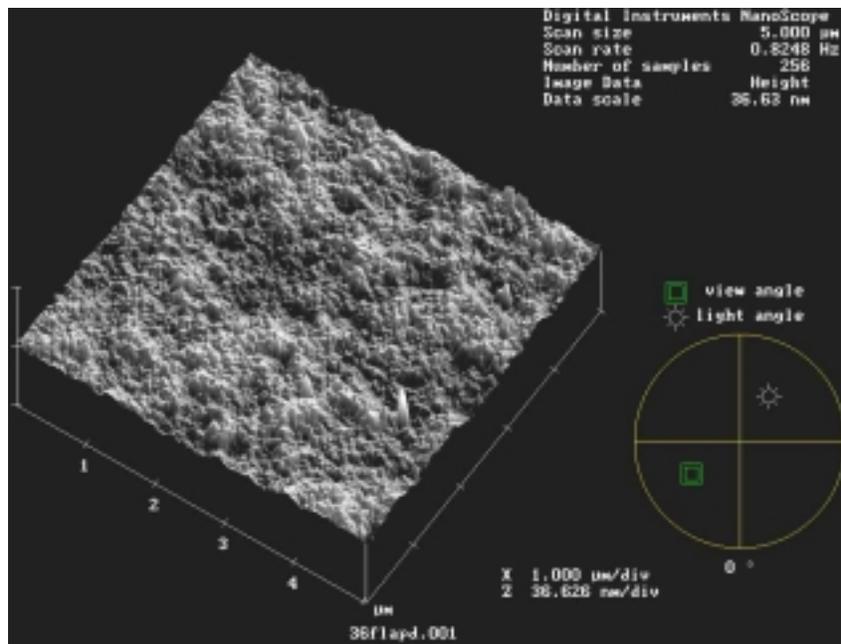


Figure 7. AFM scan of the underlying, bottom surface of the same poly1 plate scanned in Figure 6.

High speed cameras and laser vibrometers have been previously used as visualization aides for polysilicon microstructure movement [13]. Since material properties and (micro)geometries are subject to manufacturing variations, it is necessary to establish metrology parameters (or at least a sufficient number of indicators) for each wafer or fabrication facility. To this end each wafer needs to incorporate one or more test structures, on which specialized characterization tests are performed routinely to characterize the particular fabrication process. MNTV characterization tools and methods are pushing the envelope in terms of MEMS reliability. This data is then put into a solid mechanics analysis that then produces a reliability estimate. It is anticipated that all commercial foundries will perform these standardized measurements and supply the data to the customer along with the MEMS chips.

6. ACKNOWLEDGEMENTS

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